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12EC077

**M.Tech. Degree Examination, June/July 2013**

## Synthesis and Optimization of Digital Circuits

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions.**

1. a. Draw the Y chart for different level of abstraction and synthesis. Explain different levels briefly. (10 Marks)  
 b. Explain the different phases in the design of micro-electronic circuits. Give the block representation. (10 Marks)
2. a. Define the following terms with respect to concept of graph theory and give an example for each:
  - i) Undirected graph
  - ii) Directed graph
  - iii) Hyper graph (06 Marks)
 b. Compute the shortest path weight of the graph shown in Fig.Q2(b): (08 Marks)

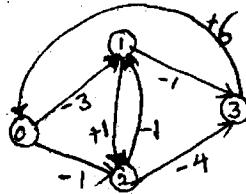


Fig.Q2(b)

- c. Consider the function  $f = ab + bc + ac$ . Compute the Boolean difference, the consensus and smoothing with respect to the variable  $a$ . Also indicate them in the cubical form. (06 Marks)
3. a. Consider the following model fragment,
 
$$xl = x + dx; \quad ul = u - (3 * x * u * dx) - (3 * y * dx); \quad yl = y + u * dx; \quad c = xl < a;$$
 Draw: i) Data flow graph, (10 Marks)  
 ii) Sequencing graph. (10 Marks)  
 b. Briefly explain control flow based transformation and block level transformation. (10 Marks)
4. a. Consider the three input, two output function  $f_1 = \overline{abc} + \overline{ab}c + a\overline{b}c + abc + abc$ ;  $f_2 = \overline{ab}c + a\overline{b}c$ ; Find minimum cover, irredundant cover and minimal cover, with respect to single implicant containment. Represent it using three dimensional Boolean cube. (10 Marks)  
 b. For the constraint matrix given below, obtain (i) compatibility graph, (ii) conflict graph.

$$A = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 \end{bmatrix}$$

(10 Marks)

5. a. Draw the logic network and logic network after elimination described by the following equation:
 
$$p = cl + de; \quad q = a + b; \quad r = p + \overline{a}, \quad s = r + \overline{b}; \quad t = ac + ad + bc + bd + e; \quad u = \overline{q}c + q\overline{c} + qc;$$

$$v = \overline{a}d + bd + \overline{c}d + a\overline{e}; \quad w = v; \quad x = s; \quad y = t; \quad z = u.$$
(10 Marks)  
 b. Explain briefly rule based systems for logic optimization. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- 6 a. For the state diagram shown in Fig.Q6(a), find minimum static diagram.

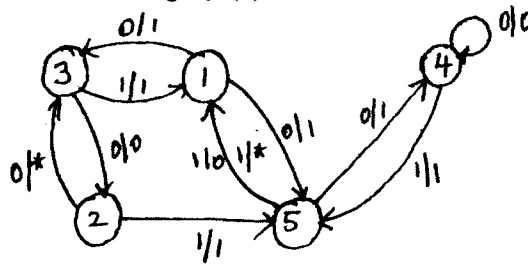


Fig.Q6(a)

- b. Explain different types of finite state machine decompositions. (10 Marks)
- 7 a. With suitable example, explain relative scheduling under timing constraints. (10 Marks)
- b. What is the need of loop folding? With suitable sequencing graph, explain loop folding. (10 Marks)
- 8 a. Explain briefly tree based matching. (08 Marks)
- b. For the module function  $m = s_1(s_2a + \bar{s}_2b) + \bar{s}_1$ ,  $(s_3c + \bar{s}_3d)$  and cluster function  $f = xy + \bar{x}z$ . Draw programmable module, module and cluster ROBDD and representation of cluster function. (12 Marks)

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